VRIJE UNIVERSITEIT BRUSSEL

The faculty of Engineering of the Vrije Universiteit Brussel invites you to attend the public defense leading to the degree of

DOCTOR OF ENGINEERING SCIENCES

of **Pratap Tumkur Renukaswamy**

The public defense will take place on **Wednesday 8th February 2023 at 4:00pm** in room **D.2.01** (Building **D**, Brussels Humanities, Sciences & Engineering Campus)

To join the digital defense, please click here
Meeting ID: 314 588 388 20
Passcode: oAkhu3

PLL MODULATION AND MIXED-SIGNAL CALIBRATION TECHNIQUES FOR FMCW CHIRP SYNTHESIS

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Abstract of the PhD research

Radar sensors have moved in the past decade from bulky systems to integrated solutions, driven by many applications in varying domains. Radar sensors are key components in self-driving cars to provide robust sensing capabilities in every weather condition. They allow contactless monitoring of vital signs such as breathing and heart rate. One of the latest applications is gesture recognition in recent smartphones.

The signals used in radar sensors are modulated signals: Frequency-Modulated Continuous-Wave (FMCW) is today the most widely used modulation. Here a carrier frequency is linearly modulated to reach a maximum over a specified period. This waveform is called a chirp.

The key component to realize this is a frequency-chirping Phase-Locked Loop (PLL), that generates an clean sinewave of a linearly increasing frequency. Many of the key performance criteria of the radar system are determined by the quality of the generated FMCW source. Any nonlinearity in the frequency versus time curve causes errors in the detected distance and speed. Any noise in the system will prevent the detection of small targets, hidden in the noise floor. The total available bandwidth (difference between maximum and minimum frequency) that can be generated determines the range resolution of the radar, where several GHz of bandwidth are required to detect targets with cm accuracy.

To address these challenges, this thesis presents a PLL modulation architecture and circuit blocks for low-power and high-performance chirp synthesis and verified using two 28 nm CMOS prototype chips. The designs will further push the performance of the FMCW PLLs, by combining innovative mixed-signal processing and calibration techniques with Charge-Integrating Digital-to-Analog Converter (QDAC) as a key building block. The 10 GHz sub-sampling PLL prototype achieves 23 MHz/µs chirp slope with 28 kHz rms-FM-error, while consuming less than 12 mW power. The 16 GHz duty-cycled charge-pump PLL design achieves a 29 MHz/µs slope with an rms-FM-error below 41 kHz while consuming less than 16.5 mW.