VRIJE UNIVERSITEIT BRUSSEL

The faculty of Engineering of the Vrije Universiteit Brussel invites you to attend the public defense leading to the degree of

DOCTOR OF ENGINEERING SCIENCES

of **Johan Hoang-Dung Nguyen**

The public defense will take place on **Friday 13th October 2023 at 3:30pm** in room **D.2.01** (Building **D,** VUB Main Campus)

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HIGH-EFFICIENCY TRANSMITTERS FOR 5G COMMUNICATION AT MM-WAVE FREQUENCIES

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Abstract of the PhD research

The fifth generation (5G) wireless communication technology started its deployment in 2019 to meet the increasing global demands for high-speed connectivity. The radio frequency spectrum will be progressively expanded to millimeter-wave ranges to meet the growing demand for mobile broadband applications. 5G targets wireless data rates of up to 10 Gbit/s. A broad deployment of applications that are based on these high data rates is only possible if the power consumption of the transmit and receive part does not grow out of hand. In a mm-wave transceiver, the transmit part often consumes most of the energy. This doctoral work focuses on the design and calibration of digital polar transmit architectures operating at mm-wave frequencies, which could bring a high data rate for less power consumption. In a polar transmitter, the signal is split in amplitude path and a phase path. The amplitude is modulated using a so-called RF-DAC, while the phase is modulated via phase modulators.

One big design achievement of this Ph.D. work is the 60-GHz digital polar chip in 28-nm Bulk CMOS. Compared to earlier digital polar transmitters operating around 60GHz, the RF-DAC used here does not suffer from leakage from disabled cells. In this way, it is possible to modulate with a higher modulation depth. Two leakage reduction techniques have been suggested from which a patent is issued: the dynamic driver and the inverter switch. The phase modulator is a Cartesian one, using a 90 degrees hybrid, that splits the input signal into an in-phase (I) and a quadrature (Q) component, which are weighted with a very linear variable gain, made with variable-gain amplifiers (VGAs). Thanks to this phase modulator and to the leakage-mitigation improvements, this chip achieves a raw data rate of 10.52 Gb/s using a 64-QAM modulation.

The on-chip impedance matching is accomplished with transformers. In this work, a design flow based on ABCD matrices has been developed to speed up the design of these transformers. The same framework is later used to design a 140-GHz transceiver front-end with a transmit/receive switch.

Synchronization between the amplitude path and the phase path is vital in digital polar architectures. To facilitate and speed up this synchronization, a non-iterative method is proposed here. This strategy is then extended to retrieve and compensate AM-AM and AM-PM distortion from the VGAs. It is also possible to estimate the IQ imbalance of the hybrid. Higher bandwidths can be achieved by using the method to calculate an equalization filter for the phase samples.