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DOCTOR OF ENGINEERING SCIENCES

of **Rana ElKashlan**

The public defense will take place on **Monday 6th November 2023 at 5:00pm** in room **D.2.01** (Building **D**, VUB Main Campus)

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GAN-ON-SI TECHNOLOGY FOR MODERN WIRELESS COMMUNICATION SYSTEMS: OPTIMISATION INSIGHT USING RF CHARACTERISATION

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Abstract of the PhD research

The increasing complexity of modern communication systems has resulted in optimising several different technologies for each specific function. Hence, such communication systems comprise many chips. The downscaling of Si CMOS technology has allowed for a large-scale integration level that includes the integration of high-speed transceivers on the chips. Nevertheless, the low-voltage operation of CMOS technology cannot meet the requirements of high-power, high-efficiency power amplifiers. Thus, alternate materials are of interest for power amplifier applications. GaN is one promising candidate based on its ability to operate at high frequency and power levels. However, RF Front-End Modules (RF-FEMs) include high-performance switches fabricated on semi-insulating substrates. Therefore, realising the next generations of power and cost-efficient RF systems depends highly on the co-integration of the different device technologies.

The main target of this work is the optimisation of GaN-on-Si HEMTs for use in such high-performance communication systems. This thesis tackles that by first enhancing AlCu-based gate-metal stacks in a gate-first process to mitigate the plausibility of the gate resistance becoming a limitation to the cut-off frequency of the unilateral gain ($f_{\max}$). The procedure of optimising the gate-metal stack utilises small-signal RF characterisation and modelling in addition to developing a gate resistance model, which accounts for the T-shape geometry of the gate. Such modelling is necessary, given that gate resistance models and extraction methods for CMOS devices do not account for the asymmetric nature of the T-gate in GaN HEMTs. After optimising the gate-metal stack, nonlinear and large-signal characterisation, combined with small-signal equivalent circuit modelling, provide insight into the linearity trade-offs associated with varying T-gate geometries. A substantial portion of this work focuses on the compromises related to different vertical layers, namely the channel thickness and the top barrier layer. Downscaling the gate lengths below 150nm enables a higher gain, which thus facilitates superior high-frequency operation. However, shorter gate lengths may increase short-channel effects. Investigating various thinned-down barrier materials, using RF small- and large-signal characterisation, reveals the necessity of improving the device linearity for thinner top barriers by lowering the source access resistance and suppressing the gate leakage. Examining the impact of thinner channel thicknesses, in the presence of a cGaN back-barrier, on the large-signal device performance clarifies a significant trade-off between short-channel effect suppression and efficient power performance, since the rise in current collapse and dispersion negatively impacts the large-signal metrics by increasing the knee voltage and reducing the maximum current. Carefully designing a composite back-barrier can alleviate some of the on-resistance, thus enhancing the output power of thin-channel downscaled devices.

Finally, the findings of this thesis provide guidelines for GaN-on-Si technology optimisation depending on the target frequency band of operation.