VRIJE UNIVERSITEIT BRUSSEL

The faculty of Engineering of the Vrije Universiteit Brussel invites you to attend the public defense leading to the degree of

DOCTOR OF ENGINEERING SCIENCES

of **Alican Çağlar**

The public defense will take place on **Monday 26th October 2026 at 4pm** in room **D.2.01** (Building D, VUB Main Campus)

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LOW-POWER CRYOGENIC CMOS INTERFACES FOR SCALABLE QUANTUM COMPUTERS

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Abstract of the PhD research

Realizing a fault-tolerant quantum computer based on superconducting or spin quantum bits (qubits) requires millions of physical qubits operating below 100 mK in dilution refrigerators. In the early years of quantum processor research and development, qubits were controlled using room temperature electronics due to their small scale. However, with the rapid increase in the number of qubits in the last decade, the massive amount of cabling required between mK temperatures and room temperature has become a bottleneck. To overcome this limitation, CMOS electronics, the technology underlying modern microprocessors, are increasingly used in close proximity to qubits at cryogenic temperatures, such as the mK and 4 K stages of dilution refrigerators. These circuits are commonly referred to as cryogenic CMOS (cryo-CMOS). The main challenge for scalable cryo-CMOS control electronics is the very low power budget in dilution refrigerators, due to their limited cooling power.

In the first phase of this research, a system-on-chip (SoC) for qubit readout at 4 K was developed using 28 nm bulk CMOS technology. The SoC employs a full zero intermediate frequency architecture and operates in the 6-8 GHz frequency range at 4 K. The readout SoC achieves lower power consumption with a noise performance comparable to prior works.

In the second phase, CMOS circuits operating at mK temperatures were investigated. In this context, two prototypes, a DC demultiplexer and a charge-redistribution DC digital-to-analog converter (DAC) implemented in 65 nm bulk CMOS technology, have been designed to alleviate the DC wiring bottleneck for spin qubit biasing. Thanks to their low power consumption, they enable the biasing of over 100,000 qubits at 100 mK.