Substrate Noise Coupling in Analog/RF Systems

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Rising integration increases the on-chip interference and causes systems to malfunction. We propose a way to model this phenomenon and diminish its effects. The possibilities of 3D-stacking is analyzed.

Context

The consumer electronic market is mainly driven by cost reduction, which is facilitated by the increasing miniaturization of the transistors. More and more functionality is therefore integrated on the same die. This leads to the proliferation of single-chip radio implementations which are also called Systems-on-Chip (SoC).
One of the most important drawbacks of such an implementation is the substrate coupling, an on-chip interference which is caused by the fast switching of the digital circuitry and is transported by the common substrate. This interfering signal is injected into the substrate, propagates through the common substrate (this is why it is called substrate noise) and finally couples into the sensitive analog/RF receivers residing on the same die. This perturbation can severely affect the performance of these radios and can even lead to malfunction.

Goal

The purpose of this work is to give the analog designer a deep understanding about how substrate noise propagates through the substrate and how it couples into the analog circuitry.

Method

The propagation of substrate noise is complex and depends on the circuit layout. Therefore we propose to use a 3D field solver to predict the propagation of substrate noise. The isolation between the digital and analog circuitry can be enhanced by the use of guard rings. Different types of guard rings are investigated and guidelines are provided to help the designer to choose the guard ring that fits the best to his needs.

Further, the different substrate noise coupling mechanisms in a single active device are revealed. Measurements and simulations point out that the importance of the coupling mechanism is determined by the resistance of the ground interconnect.

To guarantee first silicon pass, it is mandatory to accurately predict the impact of substrate noise into the sensitive analog circuitry. To this end, a methodology is presented that combines both the strengths of the emerging 3D field solvers and the circuit simulators. A large number of examples such as a 5GHz wideband receiver are modeled with this methodology. All the examples are successfully validated with measurements.

Finally, this PhD has explored the opportunity of 3D-stacking to reduce the substrate noise coupling. Measurements and simulations have pointed out that a 3D-SoC offers 10x better substrate noise isolation than a traditional 2D-SoC.